CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of refreshing a programmed programmable conductor memory cell which includes at least a programmable conductor memory element and an access device, the method comprising:

holding the access device in a non-activated state; and

applying a potential difference between the memory element and the access device to induce leakage current to flow through the programmed memory element and across the access device.

2. The method according to claim 1, wherein the access device is a transistor having a source and a drain and the leakage current is induced to flow between the source and the drain.

3. The method according to claim 2, wherein the potential difference is applied to an anode of the memory element and the leakage current is induced by setting the anode to a higher potential than the potential at the source of the access transistor.

4. The method according to claim 3, wherein the leakage current is induced by setting a difference in potential between the anode of the memory element and the source of the access device, wherein the potential difference is greater than 0V and up to approximately +0.4 V.

5. The method according to claim 4, wherein the leakage current is induced by setting a difference in potential between the anode of the memory element and the source of the access device of approximately +0.2 V.

6. The method according to claim 1, wherein the potential difference is produced by applying a voltage to an anode of the memory element.

7. The method according to claim 6, wherein the voltage is applied continuously.

8. The method according to claim 6, wherein the voltage is applied continuously to an array of memory cells, except when a read, write, or erase operation is being performed on any memory cell in the array.

9. A method for refreshing a programmed programmable conductor memory cell which includes at least a programmable conductor memory element formed on a substrate, the method comprising:

applying a voltage to the programmed memory element to thereby induce a leakage current through the memory element and the substrate.

10. The method according to claim 9, wherein the act of applying a voltage to the programmed memory element induces a leakage current between approximately 1 and 100 picoamps.

11. The method according to claim 9, wherein the act of applying a voltage to the programmed memory element comprises applying a voltage in the range of approximately 0 V to about 5.5 V.

12. The method according to claim 9, wherein the voltage is applied continuously.

13. A method of refreshing a programmed PCRAM memory cell, the method comprising leaking current through the programmed PCRAM memory cell, wherein the current is at a level which refreshes programmed cells but does not affect non-programmed cells.

14. A method of operating an array of programmable conductor memory cells, wherein each memory cell includes a variable resistance memory element and an access device and the array includes at least one row of memory cells connected along a bit line and at least one column of memory cells connected along a word line, the method comprising:

for each bit line in the array in which no read, write or erase operations are being performed, setting the bit line at a first potential; and

applying a voltage to a common anode for each memory element in the array to set the common anode to a second potential which is greater than the first potential,

wherein the access device of each memory cell is designed such that, upon application of the voltage to the common anode when the access device is not in an activated state, a leakage current is produced through the access device of each memory cell in which the respective memory element is in a programmed state.

15. The method according to claim 14, further comprising:

activating the access device of a selected memory cell in the array;

switching the voltage at the common anode to set the common anode to the first potential; and

setting the bit line to which the selected memory cell is connected to a third potential to perform a write operation to the memory element of the selected memory cell.

16. The method according to claim 14, further comprising:

activating the access device of a selected memory cell in the array;

switching the voltage at the common anode to set the common anode to the first potential; and

setting the bit line to which the selected memory cell is connected to a third potential to perform a erase operation to the memory element of the selected memory cell.

17. The method according to claim 14, further comprising:

activating the access device of a selected memory cell in the array;

switching the voltage at the common anode to set the common anode to the first potential; and

setting the bit line to which the selected memory cell is connected to a third potential to perform a read operation to the memory element of the selected memory cell.

18. A programmable conductor memory cell comprising:

a substrate;

an access transistor formed on the substrate with a source and a drain of the access transistor being formed in the substrate,

a programmable conductor memory element formed on the substrate in electrical contact with the access transistor drain;

wherein the access transistor is formed such that application of a potential difference between the memory element and the access transistor source induces a leakage current to flow through the memory element and between the source and drain of the access transistor when the memory element is in a programmed state and the access transistor is in a non-activated state.

19. The memory cell according to claim 18, wherein the access transistor has a threshold activation voltage so as to enable a leakage current in the range of about 1-100 picoamps to flow through the memory element and between the source and the drain when the memory element is in a programmed state, the access transistor is in a non-activated state, and a potential difference up to about 0.4 V is produced between the memory element and the source of the access transistor.

20. The memory cell according to claim 18, wherein

the programmable conductor memory element includes a first electrode and a second electrode;

the second electrode is in electrical contact with the access transistor drain;

the memory cell further comprises a potential source connected to the first electrode to produce the potential difference between the first electrode and the access transistor source.

21. The memory cell according to claim 20, wherein the potential source connected to the first electrode is switchable between at least two different voltage levels.

22. A programmable conductor memory cell comprising:

a substrate; and

a programmable conductor memory element formed in electrical contact with the substrate,

wherein the substrate is formed such that when the memory element is in a programmed state, application of a potential difference between the memory element and the substrate induces a leakage current through the memory element and through the substrate.

23. The memory cell according to claim 22, wherein

the memory element includes a first electrode and a second electrode; and

the substrate includes

a first well of a first conductivity type in electrical contact with the second electrode, and

a second well of a second conductivity type formed surrounding the first well, the second well having a depth of less than about 4000 Å,

wherein a remaining thickness of the substrate surrounding the second well is of the first conductivity type; and

application of a potential difference between the first electrode of the memory element and the substrate when the memory element is in a programmed state induces a leakage current which flows from the first electrode through the memory element, through the first well, through the second well, and then through the remaining thickness of the substrate.

24. The programmable conductor memory cell according to claim 23, wherein the first conductivity type is n-type, the second conductivity type is p-type, the first electrode is an anode, and the second electrode is a cathode.

25. The memory cell according to claim 23, further comprising:

an access transistor formed on the substrate, wherein the first well serves as a drain of the access transistor; and

a voltage source connected to the first electrode,

wherein when the memory element is in a programmed state, application of a voltage from the voltage source to the first electrode enables the leakage current to flow from the first electrode through the memory element, through the first well, through the second well, and then through the remaining thickness of the substrate.

26. An array of programmable conductor memory cells, comprising:

a substrate;

a plurality of programmable conductor memory cells formed on the substrate and arranged in rows and columns, wherein each row of memory cells is connected along a respective bit line and each column of memory cells is connected along a respective word line, wherein each memory cell comprises:

an access transistor formed on the substrate with a source and a drain of the access transistor being formed in the substrate, and

a programmable conductor memory element formed on the substrate in electrical contact with the access transistor drain;

wherein the access transistor is formed such that application of a potential difference between the respective memory element and the access transistor source induces a leakage current to flow through the memory element and between the source and drain of the access transistor when the memory element is in a programmed state and the access transistor is in a non-activated state.

27. The array according to claim 26, wherein the access transistor of each memory cell has a threshold activation voltage so as to enable a leakage current in the range of about 1-100 picoamps to flow through the respective memory element and between the source and the drain of the respective access transistor when the respective memory element is in a programmed state, the respective access transistor is in a non-activated state, and a potential difference up to about 0.4 V is produced between the respective memory element and the source of the respective access transistor.

28. The array according to claim 26, further comprising

a common first electrode for each memory element in the array formed as a single cell plate, wherein each memory element further includes a respective second electrode provided in electrical contact with the access transistor drain; and

a voltage source connected to the common anode to produce the potential difference between each respective memory element and the corresponding access transistor source.

29. The array according to claim 28, wherein the voltage source connected to the common anode is switchable between at least two different voltage levels.

30. An array of programmable conductor memory cells, comprising:

a substrate;

a plurality of memory cells formed on the substrate and arranged in rows and columns, wherein each row of memory cells is connected along a respective bit line and each column of memory cells is connected along a respective word line, wherein each memory cell comprises a programmable conductor memory element formed in electrical contact with the substrate,

wherein the substrate is formed such that when at least one of the memory elements in the array is in a programmed state, application of a potential difference between each of the at least one programmed memory element and the substrate induces a leakage current through each of the at least one programmed memory element and through the substrate.

31. The array according to claim 30, further comprising:

a cell plate forming a common electrode to each memory element in the array; and

a voltage source connected to the common anode, wherein application of a voltage from the voltage source to the cell plate induces a leakage current to flow through each of the at least one programmed memory element in the array and through the substrate.

32. The array according to claim 30, wherein

each memory element in the array includes a first electrode and a second electrode; and

the substrate includes

a first well of a first conductivity type for each memory cell, each first well being in electrical contact with the second electrode of the respective memory element of the corresponding memory cell, and

a common second well of a second conductivity type formed surrounding each of the respective first wells, the second well having a depth of less than about 4000 Å,

a remaining thickness of the substrate surrounding the common second well is of the first conductivity type; and

application of a potential difference between the first electrode of each of the at least one programmed memory element and the substrate induces a leakage current which flows from the first electrode through each respective programmed memory

element, through the corresponding first well, through the second well, and then through the remaining thickness of the substrate.

33. The array according to claim 32, wherein the first conductivity type is n-type, the second conductivity type is p-type, the first electrode of each memory element is an anode formed as a common cell plate to each memory element in the array, and the second electrode of each memory element is a cathode.

34. The array according to claim 32, wherein

the first electrode of each memory element in the array is a common electrode formed as a cell plate for each memory element in the array,

each memory cell further comprises a respective access transistor formed on the substrate, such that the respective first well serves as a drain of the access transistor,

a voltage source connected to the common first electrode, and

application of a voltage from the voltage source to the common first electrode enables the leakage current to flow from the common first electrode through each of the at least one programmed memory element, through the corresponding first well, through the second well, and then through the remaining thickness of the substrate.

35. The array according to claim 30, wherein

each memory element in the array includes a first electrode and a second electrode; and

the substrate includes

a first well of a first conductivity type for each memory cell, each first well being in electrical contact with the second electrode of the respective memory element of the corresponding memory cell, and

for each first well, a second well of a second conductivity type surrounding the respective first well, each second well having a depth of less than about 4000 Å,

a remaining thickness of the substrate surrounding each of the second wells is of the first conductivity type; and

application of a potential difference between the first electrode of each of the at least one programmed memory element and the substrate induces a leakage current which flows from the first electrode through each respective programmed memory element, through the corresponding first well, through the corresponding second well, and then through the remaining thickness of the substrate.

36. The array according to claim 35, wherein the first conductivity type is n-type, the second conductivity type is p-type, the first electrode of each memory element is an anode formed as a common cell plate to each memory element in the array, and the second electrode of each memory element is a cathode.

37. The array according to claim 35, wherein

the first electrode of each memory element in the array is a common electrode formed as a cell plate for each memory element in the array,

each memory cell further comprises a respective access transistor formed on the substrate, such that the respective first well serves as a drain of the access transistor,

a voltage source connected to the common first electrode, and

application of a voltage from the voltage source to the common first electrode enables the leakage current to flow from the common first electrode through each of the at least one programmed memory element, through the corresponding first well, through the second well, and then through the remaining thickness of the substrate.

38. A processing system, comprising:

a processor for receiving and processing data;

at least one memory array for exchanging data with the processor; and

a memory controller for managing memory access requests from the processor to the at least one memory array,

wherein each of the at least one memory array includes:

a substrate;

a plurality of programmable conductor memory cells formed on the substrate and arranged in rows and columns, wherein each row of memory cells is connected along a respective bit line and each column of memory cells is connected along a respective word line, wherein each memory cell comprises:

an access transistor formed on the substrate with a source and a drain of the access transistor being formed in the substrate, and

a programmable conductor memory element formed on the substrate in electrical contact with the access transistor drain;

wherein the access transistor is formed such that application of a potential difference between the respective memory element and the access transistor source induces a leakage current to flow through the memory element and between the source and drain of the access transistor when the memory element is in a programmed state and the access transistor is in a non-activated state.

39. The processing system according to claim 38, wherein each array further comprises:

a common first electrode for each memory element in the array formed as a single cell plate, wherein each memory element further includes a respective second electrode provided in electrical contact with the access transistor drain; and

a voltage source connected to the common anode to produce the potential difference between each respective memory element and the corresponding access transistor source.

40. A processing system, comprising:

a processor for receiving and processing data;

at least one memory array for exchanging data with the processor; and

a memory controller for managing memory access requests from the processor to the at least one memory array,

wherein each of the at least one memory array includes:

a substrate;

a plurality of memory cells formed on the substrate and arranged in rows and columns, wherein each row of memory cells is connected along a respective bit line and each column of memory cells is connected along a respective word line, wherein each memory cell comprises a programmable conductor memory element formed in electrical contact with the substrate,

wherein the substrate is formed such that when at least one of the memory elements in the array is in a programmed state, application of a potential difference between each of the at least one programmed memory element and the substrate induces a leakage current through each of the at least one programmed memory element and through the substrate.

41. The processing system according to claim 30, wherein each of the at least one array further comprises:

a cell plate forming a common electrode to each memory element in the respective array; and

a voltage source connected to the common anode, wherein application of a voltage from the voltage source to the cell plate induces a leakage current to flow through each of the at least one programmed memory element in the respective array and through the substrate.